

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,803,826 B2
APPLICATION NO. : 10/763038
DATED : October 12, 2004
INVENTOR(S) : Tyler J. Gomm, Frank Aljano and Howard C. Kirsch

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

	<u>Reads</u>	<u>Should Read</u>
On the title page second page Item (56), Jang Reference	"Jang, Seong-Jin et al., A Compact Ring Delay Line for High Speed Synchronous DRAM, IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1998, pp. 60-61."	--Jang, Seong-Jin et al., "A Compact Ring Delay Line for High Speed Synchronous DRAM," IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1998, pp. 60-61.--
On the title page second page Item (56) Takai Reference	"Takai, Yasuhiro et al., A 250Mb/s/pin 1 Gb Double Data Rate SDRAM with a Bi-Directional Delay and an Inter-Bank Shared Redundancy Scheme, 1999."	--Takai, Yasuhiro et al., "A 250Mb/s/pin 1 Gb Double Data Rate SDRAM with a Bi-Directional Delay and an Inter-Bank Shared Redundancy Scheme," 1999.--
Item (57), Line 10	"in put clock signal"	--input clock signal--
Column 3, Line 18	"at a time T0,"	--at a time T0,--
Column 3, Line 19	"variable delay VD as a"	--variable delay VD has a--
Column 3, Line 62	"each cycle of the CLK"	--in each cycle of the CLK--
Column 5, Line 15	"present invention a delay-"	--present invention, a delay- --
Column 5, Line 39	"and also coupled"	--and is also coupled--
Column 5, Line 65	"a delayed clock signal."	--of a delayed clock signal.--
Column 5, Line 66	"FIG. 6 a functional"	--FIG. 6 is a functional--
Column 6, Line 37	"receives CLKBUF signal"	--receives the CLKBUF signal--

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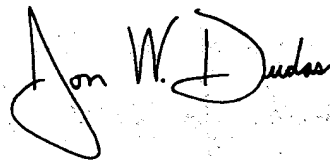
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Column 8, Line 17	"edge is all the CLKBUF"	--edges of the CLKBUF--
Column 8, Line 60	"having a rising-edges"	--having rising-edges--
Column 9, Line 5	"substrate in which the"	--substrate in the--
Column 9, Line 21	"of the clkosc signal"	--of the CLKOSC signal--
Column 9, Line 31	"606 the operating"	--606 operating in--
Column 9, Line 33	"having been with rising"	--having rising--
Column 9, Line 40	"detail."	--in detail.--
Column 11, Line 44	"two 32 bits words"	--two 32-bit words--
Column 11, Line 53	"received N/2 bits words"	--received N/2 bit words--
Column 14, Line 7	"being resetresponsive"	--being reset responsive--
Column 14, Line 65	"clock signal an develop"	-- clock signal and develop --

Signed and Sealed this

Tenth Day of October, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office